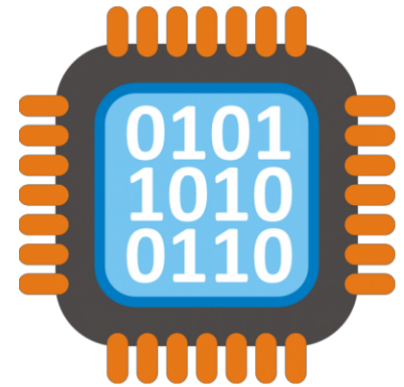


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Secure Assembly Coding

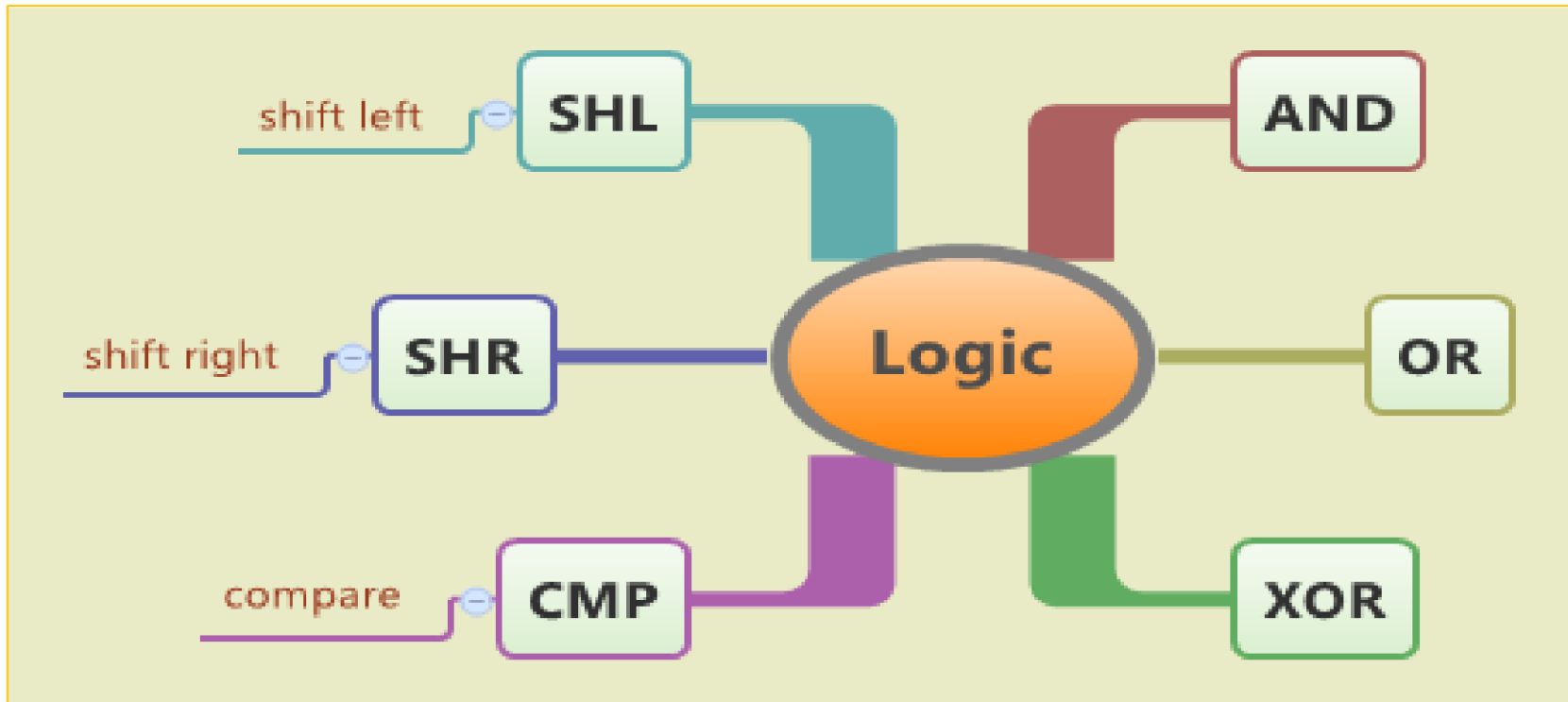
Week # 8 Lectures

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Department of Cybersecurity,



8086 Instruction Set

Group 3 : Bit Manipulation Instructions (logical).



Arithmetic Instructions:

AND, OR, XOR, NOT, TEST, SHL, SHR, SAL, SAR, ROL, ROR, RCL, RCR

8086 Instruction Set

Group 3 : Bit Manipulation Instructions (logical).

Logicals

NOT mem/reg	NOT byte or word	→ <i>One's complement</i>
AND a, b	AND byte or word	
OR a, b	OR byte or word	
XOR a, b	Exclusive OR byte or word	
TEST a, b	Test byte or word	

Shifts

SHL/SAL mem/reg, CNT	Shift logical/arithmetic left byte or word
SHR/SAR mem/reg, CNT	Shift logical/arithmetic right byte or word

Rotates

ROL mem/reg, CNT	Rotate left byte or word
ROR mem/reg, CNT	Rotate right byte or word

a = "reg" or "mem," b = "reg" or "mem" or "data," CNT = number of times to be shifted.
If CNT > 1, then CNT is contained in CL. Zero or negative shifts and rotates are illegal.
If CNT = 1 then CNT is immediate data. Up to 255 shifts are allowed.

8086 Instruction Set

Group 3 : Bit Manipulation Instructions (logical).

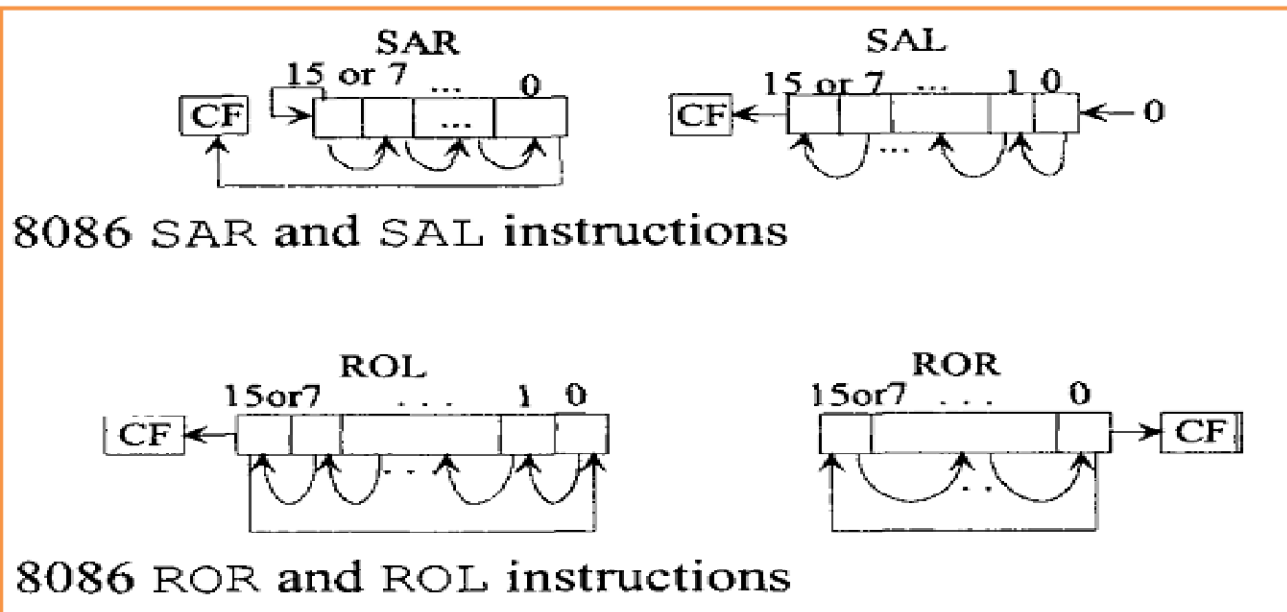
EX: TEST CL, 05H

Logically ANDs (CL) with 00000101. Does not store the result in CL, All flags are affected.

EX: Let AL=0111 1111 =7FH,

TEST AL, 80H; AL=7FH (unchanged), ZF=1 since (AL) AND (80H)=00H; SF=0; PF=1

EX: MOV CL,2 ; Shift count 2 is moved into CL
SHR DX,CL; Logically shifts (DX) twice to right



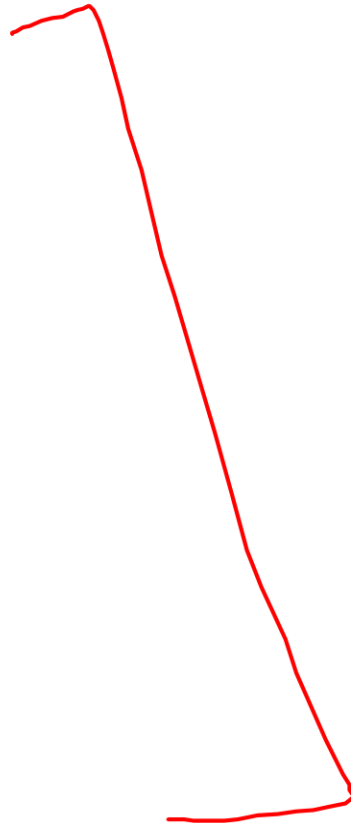
Bitwise instructions

- **Logical Instructions**

- **AND** : Turns off specific bits (used with masking) .
- **TEST** : Same as AND , but does not change destination .
- **OR** : Turns on specific bits .
- **NOT** : Complement all the bits .
- **XOR** : Complement specific bits .

Shift and Rotate Instructions

- SHR : Shift Right
- SAR : Shift Arithmetic Right
- SHL : Shift Left
- SAL : Shift Arithmetic Left
- ROL : Rotate Left
- ROR : Rotate Right
- RCL : Rotate Carry Left
- RCR : Rotate Carry Right



Logical Instructions

AND Truth Table

Inputs		Output
A	B	$Y = A.B$
0	0	0
0	1	0
1	0	0
1	1	1

OR Truth Table

Inputs		Output
A	B	$Y = A+B$
0	0	0
0	1	1
1	0	1
1	1	1

XOR Truth Table

Inputs		Output
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

NAND Truth Table

Inputs		Output
A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

www.geekyshows.com

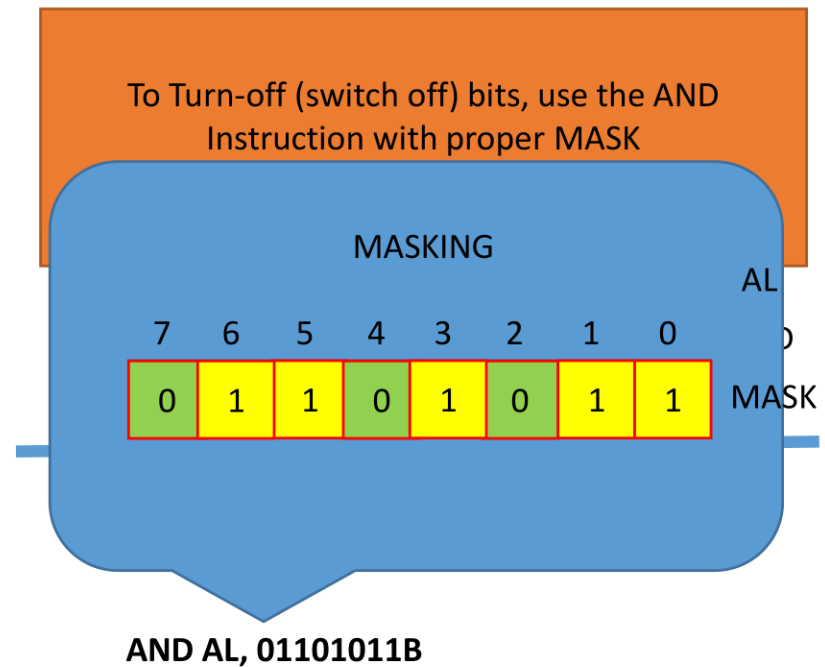
Logical Instructions

Given the AL Register as follows:

7	6	5	4	3	2	1	0
1	1	0	1	0	0	1	1

Perform the following Tasks on the AL Register:

1) Turn off bits numbers 2, 4, 7



Given the AL Register as follows:

7	6	5	4	3	2	1	0
1	1	0	1	0	0	1	1

Perform the following Tasks on the AL Register:

1) Turn on bits numbers 3, 5, 6

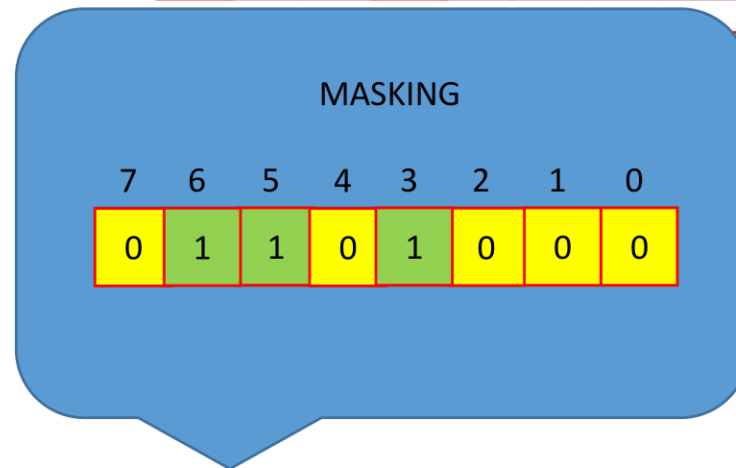
To Turn-on (switch on) bits, use the OR Instruction with proper MASK
Use 1 under the bit to turn on in the mask

7	6	5	4	3	2	1	0
1	1	0	1	0	0	1	1

AL

OR

MASK



OR AL, 01101000B

XOR Truth Table

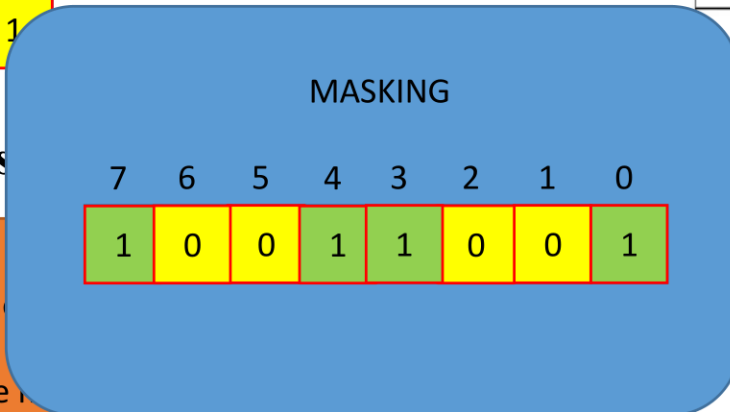
Inputs		Output
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Given the AI Register as follows:

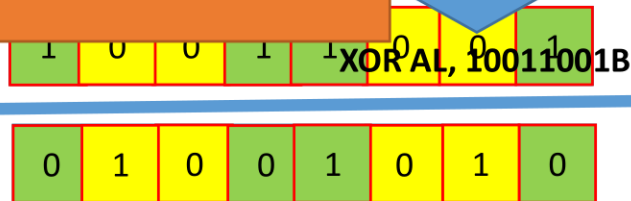


3. Switch (Complement) bits

To Complement the value of a bit, use the
Instruction with proper MASK
Use 1 under the bit to complement in the



XOR



Switch is also called toggle

Cont.

AL =

7	6	5	4	3	2	1	0
1	1	0	1	0	0	1	1

2) Turn on first 4 bits (0,1,2,3)
OR AL, 00001111B

1	1	0	1	1	1	1	1
---	---	---	---	---	---	---	---

3) Turn off last 4 bits (4,5,6,7)
AND AL, 00001111B

0	0	0	0	1	1	1	1
---	---	---	---	---	---	---	---

AL contains the same original value after the test... It is unchanged

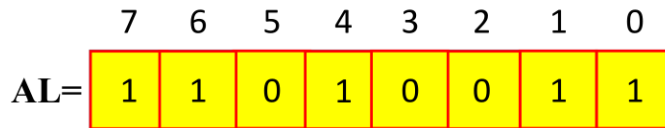
The results in AL is that the first 4 bits are on

Now, to switch off the last 4 bits (4,5,6,7)
We use the AND instruction with the mask

0	0	0	0	1	1	1	1
---	---	---	---	---	---	---	---

Cont.

4) Else IF bit 3 is 1 then Complement the last 4 bits



ON: XOR AL,11110000B



EXIT: MOV AX,4C00H
INT 21H

To complement the last 4 bits (4,5,6,7)
We use the XOR instruction with the mask

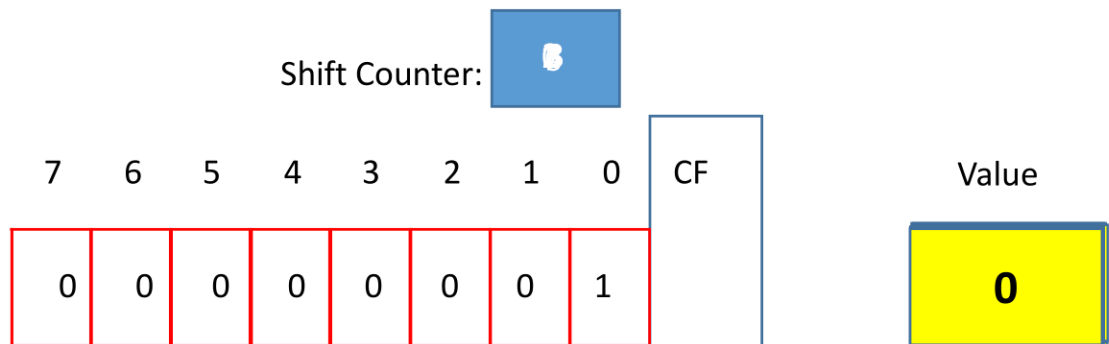


Shift Right

Syntax: SHR Register, Bits to be shifted

Example: Mov AL, 173
SHR AL, 8

; Note every shift to the right is a division by 2

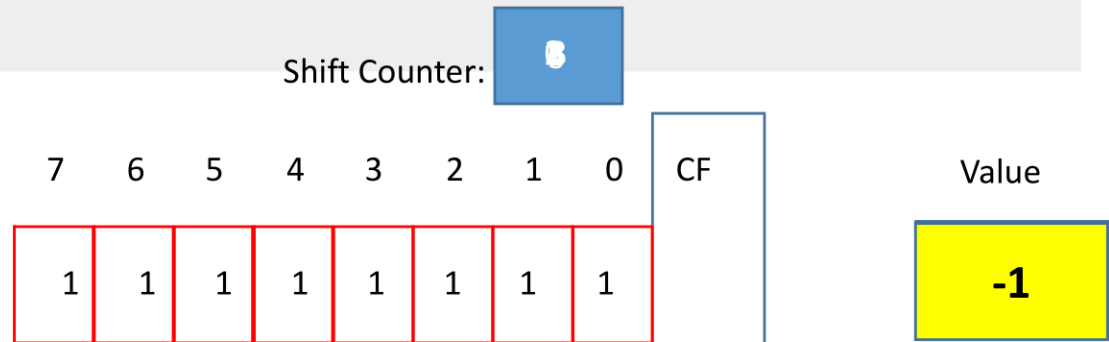


SAR : Shift Arithmetic Right

The SAR instruction stands for 'Shift Arithmetic Right'. This instruction shifts the mentioned bits in the register to the right side one by one, but instead of inserting the zeroes from the left end, the MSB is restored. The rightmost bit that is being shifted is stored in the Carry Flag (CF). **Works with Signed Numbers.**

Syntax: SAR Register, Bits to be shifted

Example: Mov AL, -80
SAR AL, 8



SHL : Shift Left

The SHL instruction is an abbreviation for 'Shift Left'. This instruction simply shifts the mentioned bits in the register to the left side one by one by inserting the same number (bits that are being shifted) of zeroes from the right end. The leftmost bit that is being shifted is stored in the Carry Flag (CF).

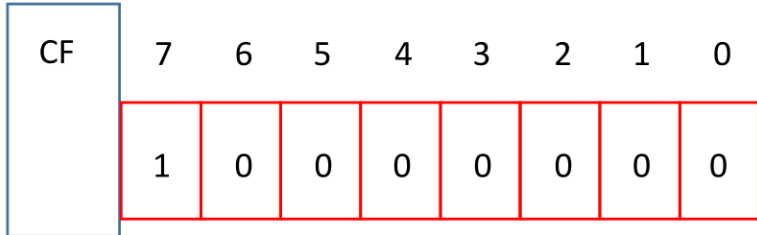
Syntax: SHL Register, Bits to be shifted

```
MOV AL, 5
```

Example: SHL AL, 8 ; Note every shift to the left is similar to multiply by 2

Shift Counter:

8



Value

0

SAL : Shift Arithmetic Left

The SAL instruction is an abbreviation for 'Shift Arithmetic Left'. This instruction is the same as SHL.

Syntax: SAL Register, Bits to be shifted

Example: SAL CL, 3

ROL : Rotate Left

The ROL instruction is an abbreviation for 'Rotate Left'. This instruction rotates the mentioned bits in the register to the left side one by one such that leftmost bit that is being rotated is again stored as the rightmost bit in the register, and it is also stored in the Carry Flag (CF).

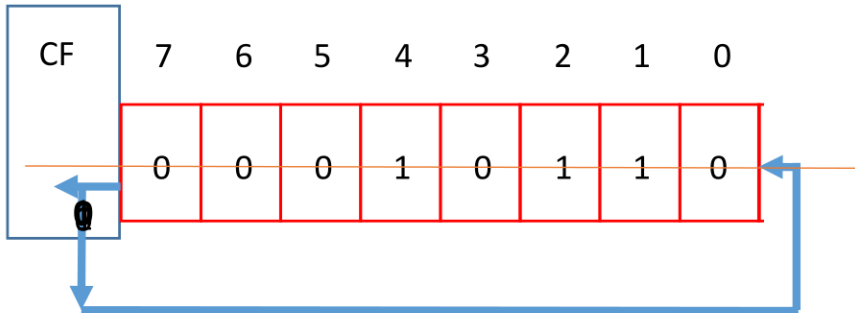
Syntax: ROL Register, Bits to be shifted

Example: ROL AH, 8



Shift Counter:

8



Value

44

ROR : Rotate Right

The ROR instruction stands for 'Rotate Right'. This instruction rotates the mentioned bits in the register to the right side one by one such that rightmost bit that is being rotated is again stored as the MSB in the register, and it is also stored in the Carry Flag (CF).

Syntax: `ROR Register, Bits to be shifted`

Example: `ROR AH, 4`

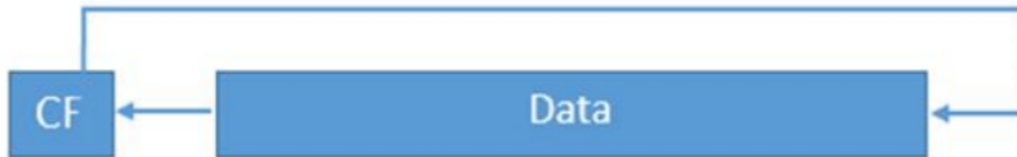


RCL : Rotate Carry Left

This instruction rotates the mentioned bits in the register to the left side one by one such that leftmost bit that is being rotated it is stored in the Carry Flag (CF), and the bit in the CF moved as the LSB in the register.

Syntax: `RCL Register, Bits to be shifted`

Example: `RCL CH, 1`

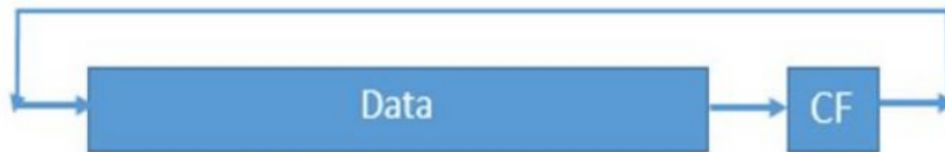


RCR : Rotate Carry Right

This instruction rotates the mentioned bits in the register to the right side such that rightmost bit that is being rotated it is stored in the Carry Flag (CF), and the bit in the CF moved as the MSB in the register.

Syntax: `RCR Register, Bits to be shifted`

Example: `RCR BH, 6`



Assembly-BIT-Wise-instructions.pptx - PowerPoint

original source code

```

01 ; multi-segment executable file temp
02
03 data segment
04 ; add your data here!
05 pkey db "press any key...$"
06 ends
07
08 stack segment
09 dw 128 dup(0)
10 ends
11
12 code segment
13 start:
14 ; set segment registers:
15 mov ax, data
16 mov ds, ax
17 mov es, ax
18
19 mov bl, 0f2h
20 add bl, 0f1h
21
22 mov al, 00101100B
23 RCL AL, 8
24

```

watch: AX

word byte

hex: 00

bin: 00000000

oct: 000

decimal 8 bit

unsigned: 0

signed: 0

ascii:

CF 0 ZF 0 SF 0 OF 0 PF 0 AF 0 IF 1 DF 0

analyse

emulator: noname.exe

file math debug view external virtual devices virtual drive help

Load reload step back single step run step delay m:

registers	H	L	0722:0000	0722:0000
AX	00	00	07220: B8 184	MOV AX, 00710h
BX	00	00	07221: 10 016	MOV DS, AX
CX	01	AE	07222: 07 007 BEEP	MOV ES, AX
DX	00	00	07223: 8E 142	MOV BL, 0F2h
CS	0722		07224: D8 216	ADD BL, 0F1h
IP	0000		07225: 8E 142	MOV AL, 02Ch
SS	0712		07226: C0 192	RCL AL, 1
SP	0100		07227: B3 179	RCL AL, 1
BP	0000		07228: F2 242	RCL AL, 1
SI	0000		07229: 80 128	RCL AL, 1
DI	0000		0722A: C3 195	RCL AL, 1
DS	0700		0722B: F1 241	RCL AL, 1
ES	0700		0722C: B0 176	RCL AL, 1
			0722D: 2C 044	RCL AL, 1
			0722E: D0 208	MOV DX, 00000h
			0722F: D0 208	MOV AH, 09h
			07230: D0 208	INT 021h
			07231: D0 208	MOV AH, 01h
			07232: D0 208	INT 021h
			07233: D0 208	MOV AX, 04C00h
			07234: D0 208	INT 021h
			07235: D0 208	NOP
			07236: D0 208	NOP
			07237: D0 208	NOP
			07238: D0 208	...

CF 7 6 5 4 3 2 1 0 Value

4 24 27 0 0 0 1 44 28 25

24
25
26
27
28
29
30
01

```

lea dx, pkey
mov ah, 9
int 21h ; output string at ds:dx

; wait for any key...
mov ah, 1
| 011

```

SLIDE 19 OF 20 ENGLISH (UNITED STATES)

**See other examples in
the separate ppt file
uploaded into Moodle**

More Example_2

Main Sources for these slides

- *K. R. Irvine. Assembly Language for x86 Processors, 8th edition, Prentice-Hall (Pearson Education), June 2019. ISBN: 978-0135381656.*
- *B. Dang, A. Gazet, E. Bachaalany. Practical Reverse Engineering: x86, x64, ARM, Windows® Kernel, Reversing Tools, and Obfuscation. John Wiley & Sons, June 2014. ISBN: 978-1-118-78731-1*
- *Qasem Abu Al-Haija, “Microprocessor Systems”, King Faisal University, Saudi Arabia*
- *Ghassan Issa, “Computer Organization”, Petra University, Jordan.*

Thank you